

REMARKS

The above amendment is made in response to the Office action of April 17, 2003. Claims 1, 8, 15, 19, 20, and 22 have been amended. Claims 5, 6, 16, 21, and 23 have been cancelled. Claims 1-4, 7-15, 17-20, 22, and 24-26 are pending in the present application and stand rejected. The Examiner's reconsideration is respectfully requested in view of the above amendment and the following remarks.

The Office Action objected to the drawings stating that Figures 1-3 should be designated by the legend "Prior Art." Corrected Figures 1-3 are submitted herewith. Withdrawal of the objection to the drawings is respectfully requested.

Claims 1, 2, and 7 were rejected under 35 U.S.C. § 102(b) as being anticipated by Hagersten et al (U.S. Patent No. 5,864,671). The rejection is respectfully traversed.

As illustrated in Figure 6 of Hagersten, Hagersten discloses a directory cache 604 located in the directory unit 600. In the present invention, the directory cache is "disposed within the functionality of a corresponding coherence controller," as claimed in amended claim 1 and illustrated in Figure 1. Hagersten does not disclose "said at least one directory cache disposed within the functionality of a corresponding coherence controller."

Amended claim 1 further provides "at least one single-bit sharing history indicator corresponding to each of at least one memory directory, said at least one single-bit sharing history indicator indicating a first value or a second value, wherein the first value indicates that only one node maintains a cached copy of the corresponding line of main memory and the second value indicates that more than one node maintains a cached copy of the corresponding line of main memory." The Office Action admits that Hagersten does not disclose a single-bit sharing history indicator.

The reference of Guzovskiy et al (U.S. Patent No. 5,752, 258) discloses an n-bit state value. The Office Action states that the state value identifies the state of access of each processor that shares access to the cache line. However, the n-bit state value is not a “single-bit sharing history indicator” that “indicat[es] a first value or a second value, wherein the first value indicates that only one node maintains a cached copy of the corresponding line of main memory and the second value indicates that more than one node maintains a cached copy of the corresponding line of main memory,” as claimed in amended claim 1. Further, as stated on page 11 of the present application, lines 10-11, the single-bit sharing history indicator is advantageous over multi-bit indicators because of its efficient use of directory space. As such, Guzovskiy does not anticipate amended claim 1.

Accordingly, amended claim 1 is believed to be patentably distinct in view of Hagersten. Dependent claims 2-4 and 7 are believed to be allowable for at least the reasons given for claim 1. Withdrawal of the rejection of claims 1-4 and 7 under 35 U.S.C. §102(b) is respectfully requested.

Claims 8, 9, and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hagersten et al (U.S. Patent No. 5,864,671) and Loewenstein et al. (U.S. Patent No. 6,141,692). The rejection is respectfully traversed.

Amended claim 8 provides, *inter alia*, “means for using the state information to select the directory cache line with the least memory directory entries for the corresponding line of main memory cached in two or more nodes and evict the directory cache line in the directory cache.” The Office Action admits that Hagersten does not teach means for using state information to evict directory cache lines in the directory cache as essentially recited in claim 1. Lowenstein uses state information to determine whether a

cache line contains valid data before informing the home directory that the cache line is to be replaced. The present invention, however, evicts the directory cache line “with the least memory directory entries for the corresponding line of main memory cached in two or more nodes,” as claimed in amended claim 8. Lowenstein does not disclose such limitations. As such, even assuming Hagersten and Lowenstein are properly combined, Hagersten and Lowenstein do not disclose at least “means for using the state information to select the directory cache line with the least memory directory entries for the corresponding line of main memory cached in two or more nodes and evict the directory cache line in the directory cache,” as claimed in amended claim 8.

Accordingly, amended claim 8 is believed to be patentably distinct and nonobvious in view of Hagersten and Lowenstein. Dependent claims 9-14 are believed to be allowable for at least the reasons given for claim 8. Withdrawal of the rejection of claims 8-14 is respectfully requested.

Claims 15-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hagersten et al (U.S. Patent No. 5,864,671) and Young et al. (U.S. Patent No. 5,860,120). The rejection is respectfully traversed.

Amended claim 15 recites, *inter alia*, “said at least one directory cache disposed within the functionality of the corresponding at least one coherence controller.” As previously mentioned, Hagersten does not disclose such limitations. Young does not disclose even “said at least one directory cache.” As such, even assuming that Hagersten and Young can be properly combined, Hagersten and Young do not disclose at least “said at least one directory cache disposed within the functionality of the corresponding at least one coherence controller,” as claimed in amended claim 15.

Accordingly, amended claim 15 is believed to be patentably distinct and nonobvious in view of Hagersten and Young. Dependent claims 17-18 are believed to be allowable for at least the reasons given for claim 15. Withdrawal of the rejection of claims 15 and 17-18 is respectfully requested.

Claims 6, 19, 22-24, and 26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hagersten et al. (U.S. Patent No. 5,864,671) and Smith et al. (U.S. Patent No. 6,055,610). The rejection is respectfully traversed.

Amended claim 19 recites, *inter alia*, “storing information describing shared behavior of the cached memory line in *a single-bit sharing history indicator*.” Similarly, amended claim 22 recites, *inter alia*, “wherein the decision to allocate is based on sharing behavior information contained in *a single-bit sharing history indicator* in the memory directory entry.” As previously mentioned, Hagersten does not disclose “a single-bit sharing history indicator. Smith also does not disclose such limitations. As such, even assuming Hagersten and Smith can be properly combined, Hagersten and Smith do not disclose at least “a single-bit sharing history indicator,” as claimed in amended claims 19 and 22.

Accordingly, amended claims 19 and 22 are believed to be patentably distinct and nonobvious in view of Hagersten and Smith. Further, claims 24 and 26 are believed to be patentable for at least the reasons given for claims 19 and 22, respectively. Withdrawal of the rejection of claims 19, 22, 24 and 26 is respectfully requested.

Claims 13, 20-21, and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hagersten et al. (U.S. Patent No. 5,864,671) and Loewenstein et al.

(U.S. Patent No. 6,141,692) and Smith et al. (U.S. Patent No. 6,055,610). The rejection is respectfully traversed.

Amended claim 20 recites, *inter alia*, “selecting for eviction a directory cache line with the least memory directory entries for the associated line of main memory cached in two or more nodes.” As previously mentioned, the Office Action admits that Hagersten does not teach means for using state information to evict directory cache lines in the directory cache as essentially recited in claim 1. Also as previously mentioned, Loewenstein does not disclose evicting a directory cache line “with the least memory directory entries for the associated line of main memory cached in two or more nodes.” Smith does not disclose even a “directory cache line.” As such, even assuming Hagersten, Loewenstein and Smith can be properly combined, Hagersten, Loewenstein and Smith do not disclose at least “with the least memory directory entries for the associated line of main memory cached in two or more nodes,” as claimed in amended claim 20.

Accordingly, amended claim 20 is believed to be patentably distinct and nonobvious in view of Hagersten and Loewenstein and Smith. Further, claim 25 is believed to be allowable for at least the reasons given for amended claim 20. Withdrawal of the rejection of claims 20 and 25 is respectfully requested.

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

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